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PhotoSound LEGION
Data acquisition and processing, 2019-01-24

This manual describes data acquisition and processing for LEGION DAQ256, DAQ128, ADC256, ADC128 Rev1.0 and Rev1.1 systems. Basic operation, expert mode operation, hardware configurations, and programming guide with SDK source code description are covered in separate documents. The use of LEGION DAQ included in PhotoSound PAFT platforms is covered by a separate user manual. This manual might be changed without notice. Registered LEGION system users will receive up-to-date versions of this manual as a part of the support plan for their system. This manual cannot be distributed without the explicit permission of PhotoSound.

Table of Contents

This manual describes the interpretation of acquired data, including the interpretation and improvement of jitter (digital matters only). Please see

- *Legion ADC operation manual.pdf* for basic operation, PC requirements, programmable filter configuration, EMI.
- *Legion ADC publication SPIE 2019.pdf* for analog signal path, noise measurements, EMI.
- *Legion ADC hardware configuration and probe interface.pdf* for channel mapping and hardware input options.

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Hardware parameters

ADC sampling rate is currently fixed at 40 MSPS (Rev1.1) or 38.5 MSPS (Rev1.0). Each odd and even ADC channel clocks are interleaved (shifted half period with respect to each other). ADC clock is twice higher 80 or 77 MHz accordingly. Each sample on the application waveform graph or file corresponds to 25 ns for R1.1. Each ADC clock is 12.5 ns for R1.1.

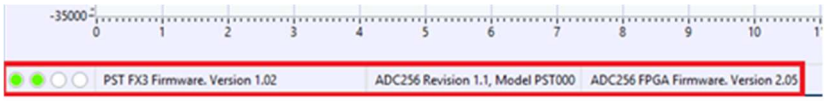

Figure 1: ADC256 or ADC128 Revision is displayed in the status bar at the bottom of application window.

ADC resolution is 12-bit signed, two's complement with 2^{12} = 4096 different values. Raw ADC data range is from -2048 to 2047. After transfer to PC, ADC data is represented 16-bit signed integer numbers with all 4 low bits zero, the data values are multiples of 16. The new range is from -32768 to 32752. Divide the data by 16 in order to restore original ADC scale from -2048 to 2047. ADC analog full scale is 2V. In order to calculate ADC input voltage, divide the numbers by 32768. To calculate the input signal, divide the result numbers by the total gain factor. Numeric gain is $10^{\text{gain dB} / 20}$. For example, 20 dB gain corresponds to 10x gain factor, 40 dB → 100x, 6 dB ~ 2x, etc. The total DAQ gain is equal to the sum of the preamplifier gain (40 dB typical) plus the ADC gain, which is programmable and might be in range from 6 to 51.875 dB.

Difference between the odd and the even channels and MAP file

Before .MAP file is loaded ADC channels are described as Ax-Cy. Ax-Cy is a physical description of the channel on ADC board; x is ADC chip number (A1 – A4 for DAQ/ADC128, A1 – A8 for single DAQ/ADC256, A1 – A32 for 4x ADC256, etc.); y is the number of the channel within ADC chip. Each ADC chip has 32 physical channels: C1 – C32.

After .MAP file is loaded, the sensor number z is added to waveform graph caption as Ax-Cy-Sz. The sensor number is the probe channel number ("logical number"), which corresponds to physical channel number.

All odd ADC channels (C1, C3, C5, … C31) are delayed with respect to even ADC channels (C2, C4, C6, … C32) by one ADC clock count = ½ sample = 12.5 ns (R1.1) for all ADC chips. ADC number Ax and the sensor number Sz have no effect on this delay. In order to find delay of the logical channels from the parity of ADC channel numbers, open .MAP file. The map file is the list of sensor numbers z sorted according to their physical channel numbers. The first sensor number z_1 in the map file corresponds to A1-C1-Sz_1, the second sensor number z_2 corresponds to A1-C2-

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Sz2, etc. **The sensors listed in .MAP file in the odd positions (z_1, z_3, z_5, …) are delayed with respect to the sensors listed in the map files in the even position (z_2, z_4, z_6, …) by one ADC clock count = ½ sample = 12.5 ns (Rev1.1).** See Figure 2 below.

In order to correctly match the data for the odd and even channels, recalculate the data with time discretization equal to ADC clock (12.5 ns for Rev1.1), i.e. double the data point number, and extrapolate missing data points for each graph. Next shift the data for odd channels to the left or even channels to the right by 12.5 ns. The resulting graph will have extrapolated point for even channels aligned with measured points for odd channels and vs versa. Such extrapolation may allow to increase effective Nyquist BW of ADC from 20 MHz to 40 MHz under assumption that photoacoustic signal in the neighbor sensor channels is correlated and they have different parity. The BW limitation in that case will be analog BW of 25 MHz, if *low power mode* option in ADC menu disabled.

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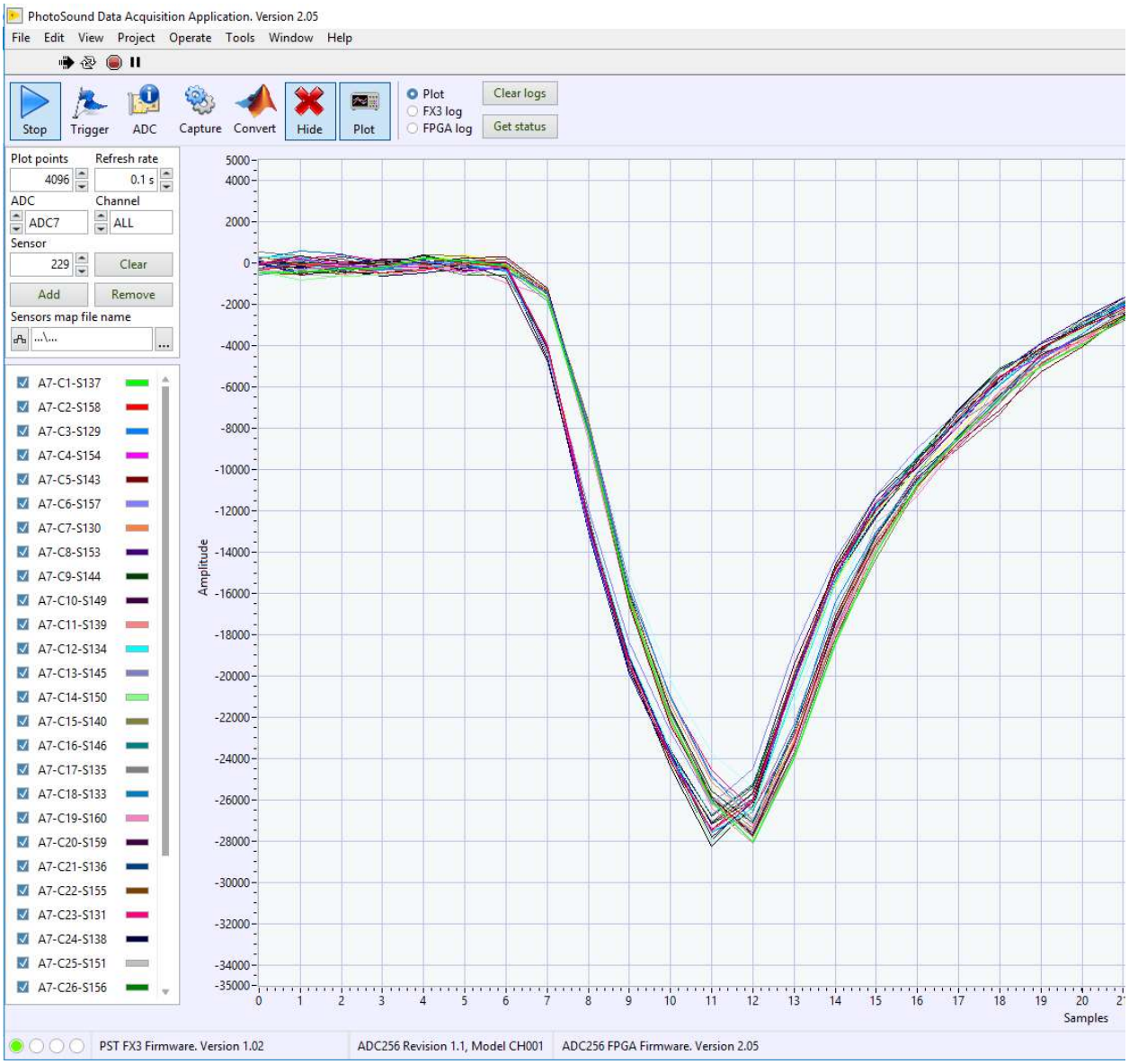

Figure 2: SE trigger output was looped back to ADC as input for all 32-channels of amplifier attached to ADC7. Trigger output signal was supplied through 80 dB attenuator, because the trigger output is 5V level. ***Notice that (a) the signal is inverted, because preamplifier is inverting, (b) all odd channels 1,3,5,… are delayed with respect to all even channels 2,4,6,… by ½ of sample or 1 ADC clock = 12.5 ns for Rev 1.1 with 80 MHz ADC clock.***

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Internal jitter

The jitter between channels in Legion ADC is well below ADC clock period 12.5 ns. In order to verify the jitter of ADC

1. connect trigger output to the analog ADC input through at least 40 dB attenuator for ADC or 80 dB attenuator for DAQ with 40 dB preamplifier, and start with small values of ADC programmable gain; see different options to inject the signal from the generator to ADC using SMA cable on Figure 3 below. ADC digital interface is described on Figure 4.
2. in the trigger menu set trigger input and output = generator
3. In order to maximize analog BW uncheck *Low power mo*de on ADC tab and choose 25 MHz *LPF cutoff frequency*, Figure 5 (4 and 5).

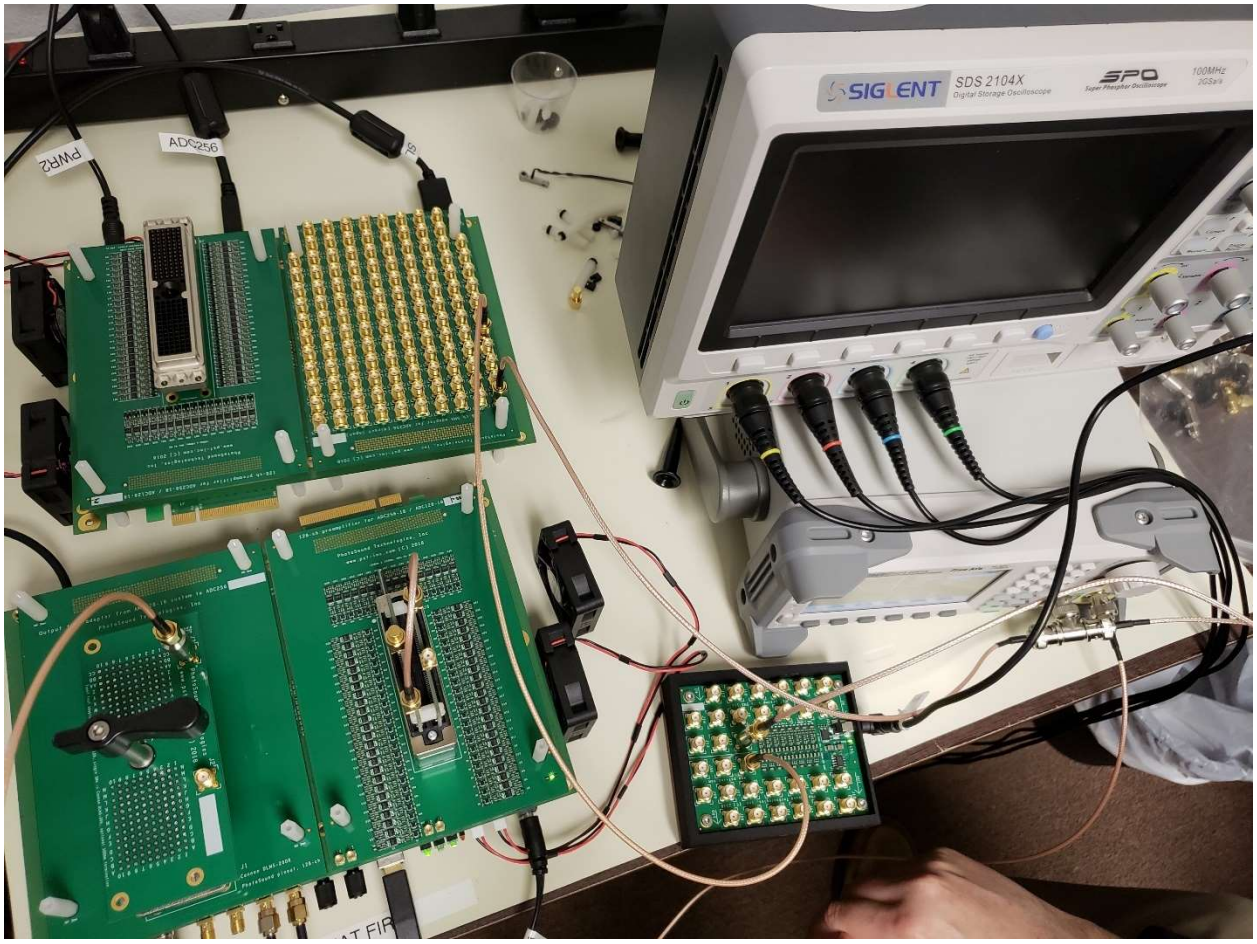

Figure 3: Physical setup for two ADC256 R1.1 boards in master-slave configuration with 512 combined channels. The slave ADC256 board (top) has 128-ch preamplifier with Cannon DLM-156 input (left) and 128-ch SMA breakout (right). The master ADC256 board (bottom) has 128-ch test adapter with Cannon DLM-260 input (left) and a standard 128-ch preamplifier with Cannon QLC-260 input (right). Cannon DLM-260 breakout input and Cannon QLC-260 amplifier input have 128-ch splitter connectors, which allows to supply the same signal to all channels for testing. One of SMA breakout board connectors have input from Flash-AMP16 (a smaller board on the bottom right) used as a preamplifier for the top ADC256. Functionally Flash-AMP16 is equivalent to AMP128, but has smaller number of channels and SMA IN and OUT connectors.

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The boards and test equipment were placed on a white antistatic mat grounded to AC outlet safety ground. ***Cannon DLM-260 breakout input receives trigger SE1 OUT signal through 40 dB attenuator (adjust ADC gain to a low level!).***

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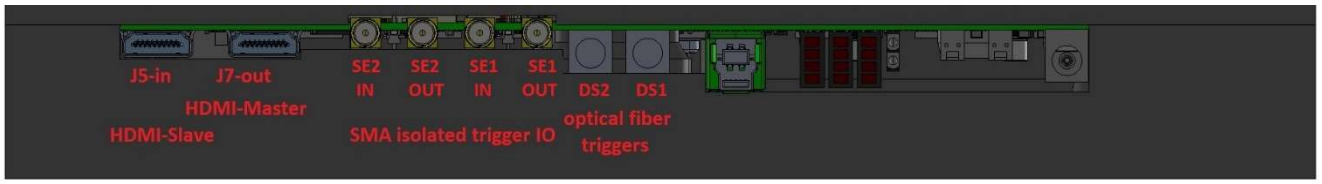

Figure 4: ADC256 front panel connectors labeled according to Input source selection.

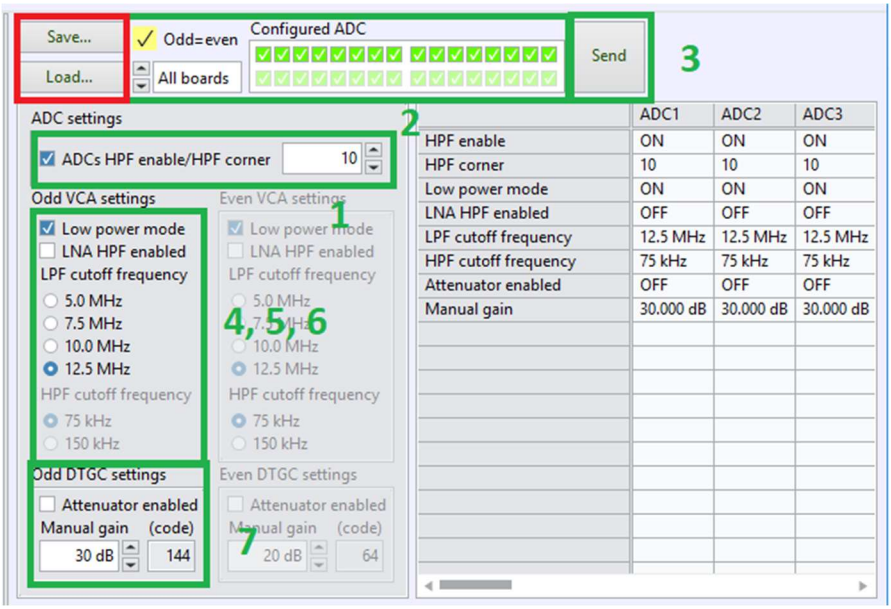

Figure 5: Use of ADC table.

4. Switch between Low-power and High-power modes. *Low-power mode* has gain range 12 – 51 dB and 12.5MHz maximal BW. High-power mode has 6 – 45 dB gain range, and up to 25 MHz BW.
5. LPF cutoff frequency can be programmed in the range 5 to 12.5 MHz for low-power mode or 10 to 25 MHz for high-power mode.

Jitter with external devices attached

Low jitter with internal clock source is the best possible result. If the jitter is measured with the trigger and the signal from the external generator with its own clock not synchronized with ADC clock, the jitter of the recorded signal will be 1 sample = 25 ns peak-to-peak. This jitter is produced by misalignment between ADC clock and generator clock. If the external low-jitter trigger source can be synchronized with ADC clock, the jitter will be limited to worse of ADC jitter or trigger source jitter. Some solid-state pulse lasers might have low-jitter trigger input. If pulse laser light output has a jitter with respect to electrical trigger input less than ADC sampling rate of 25 ns,

1. in the trigger menu set trigger input and output = generator, adjust value of period,

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2. use ADC isolated SMA trigger output as the laser trigger source.

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Convert (pending)

This example was produced for ADC256 with all eight 32-channel ADC chips running. ADC128 has four active 32-channel ADC chips. Acquired data is recorded in TDMS (*.tdms), a binary format. Information about ADC configuration is recorded in TDMS header. Decoding of data inside acquisition application is not recommended because it will affect data acquisition rate and might lead to the loss of data. The data can be decoded to a MATLAB *.mat file using the *Convert* tab.

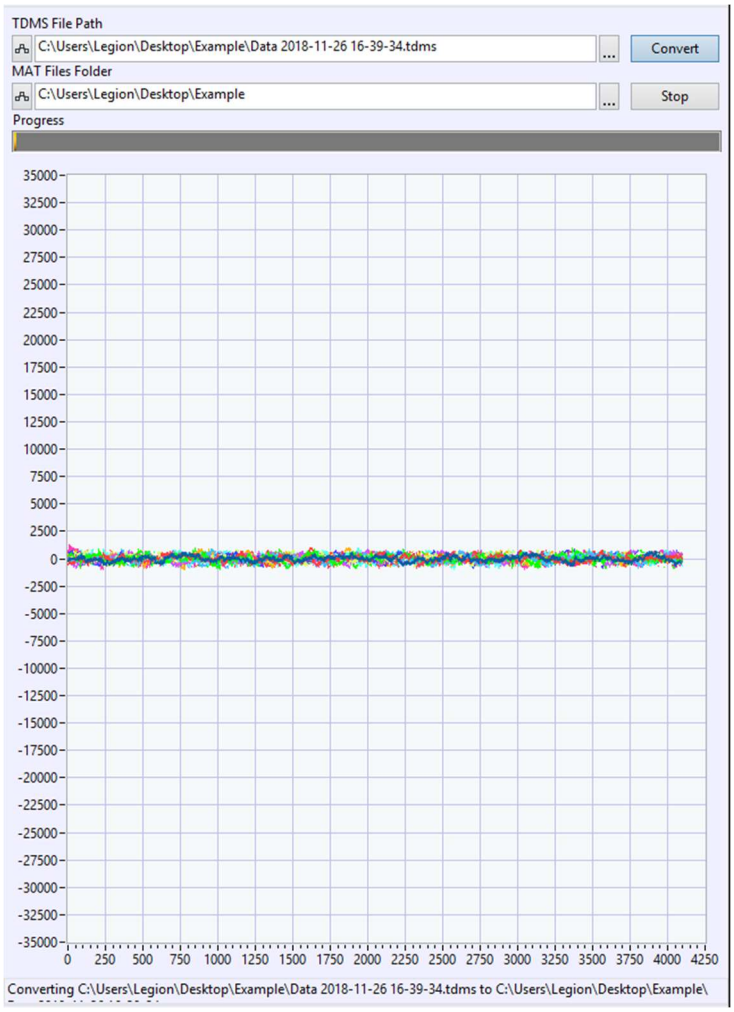

Figure 6: ADC256 data file Convert tab

To convert TDMS to .mat file

1. Choose TDMS file recorded using Convert tab in the *PhotoSound Data Acquisition Application.*
2. Choose output *.mat file name.
3. If in expert mode, choose *Packet per transfer* used to record TDMS file.

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4. Push Convert and wait until conversion is finished.
5. Use Stop to stop application or choose a new TDMS file.